



Packaging Trends Part 2

Not-So-Quiet and Very Influential Revolutions



Image: Artist Kazuhito Takadoi, courtesy of jaggedart London.

Importance of Advanced Packaging



Ack: Tom DeBonis (intel)

Source: High-End Performance Packaging 2022 – Focus on 2.5D/3D Integration report, Yole Intelligence, 2022

Importance of Advanced Packaging

3-PAGE SUMMARY – HIGH-END PERFORMANCE PACKAGING (1/3)

Market insights

High-end Packaging will be a \$7.87B market by 2027, with a 19% CAGR₂₀₂₁₋₂₀₂₇

The High-end Packaging market was worth \$2,74B in 2021 and is projected to reach \$7.87B by 2027, with a CAGR of 19% from 2021 - 2027. Breaking it down further into its end-markets, the biggest market in High-end Performance Packaging is 'Telecom & Infrastructure', with more than 50% of the market each year from 2021 - 2027. Equally important is that the fastest end-market growth in High-end Packaging is coming from 'Mobile & Consumer' and 'Automotive & Mobility', at 25% and 70% CAGR, respectively. In terms of package units, High-end Packaging is projected to experience a 24% CAGR, from 301M Units in 2021 to 1074M by 2027.

High-end Performance Packaging can also be segmented into different types of advanced packaging technology for analysis. Overall, UHD FO, HBM, 3DS, and active interposer are the biggest contributors, representing a combined market share of more than 70% by 2027.

Digital market trends demand a 3D/2.5D integration of components, which can only be addressed by High-end Packaging.

High-End Performance Packaging is increasingly implemented in HPC, cloud computing, networking, artificial intelligence, personal computing, and gaming. It is winning new market opportunities and consequently becoming a crucial solution for the More-than-Moore trend. Two of AMD's products housing 3D V-Cache – RYZEN for gaming and EPYC for servers – are a good example. In addition, UHD FO packages provided by TSMC to customers such as Cerebras, Xilinx, and GUC are hitting the market.

Within cloud computing and networking, high-end performance is required in end-systems like servers, datacenters, and base stations. Continuous demand for datacenter servers is increasing the focus on storage, computation power, and data bandwidth. Google, Facebook, Oracle, Amazon, and Alibaba are all key companies looking to own semiconductor content, thus fueling the growth of this semiconductor High-End Packaging market. The infrastructure of this market requires 2.5D and 3D packaging to integrate networking processing units and 3D stacked memories.

Advanced consumer applications, together with HPC, continue pushing TSV and in the future hybrid bonding in 3D stacked DRAM and high bandwidth memory (HBM), and are equipping GPUs with high-speed memory on 2.5D interposer platform. Embedded Si bridge is also used to interconnect HBMs to GPUs. For example, AMD released its MI200 Series accelerators for HPC and AI. GPU is the main hardware using advanced packaging technology (TSV interposer & memory) dedicated for professional & gaming PCs.

Despite Automotive & Mobility being a smaller end-market for High-end Packaging, its growth rate is one of the highest due to the price value of each unit. The strong growth of High-end Packaging in this market is mainly due to implementation in AI & robotics in automotive vehicles. Consequently, Tesla announced the Dojo D1 chip for its FSD HPC, which will help to win the robo-taxi market.

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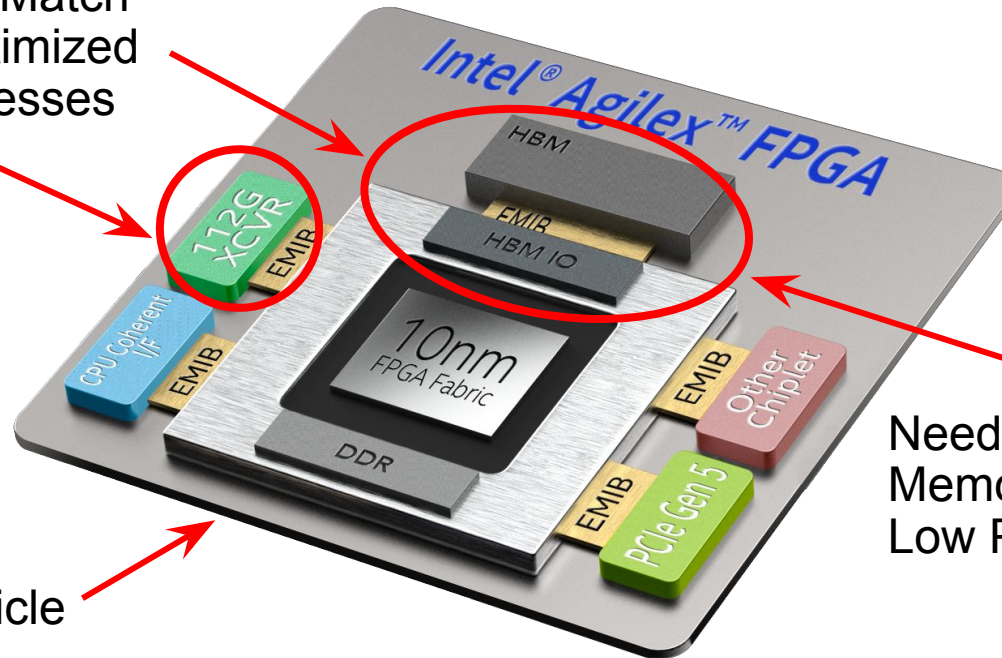
Source: High-End Performance Packaging 2022 – Focus on 2.5D/3D Integration report, Yole Intelligence, 2022

Advanced Packaging as a Vehicle for HI



Increased Interest in HI is Driven by:

Need to Mix and Match
of Diverse IP Optimized
on Different processes

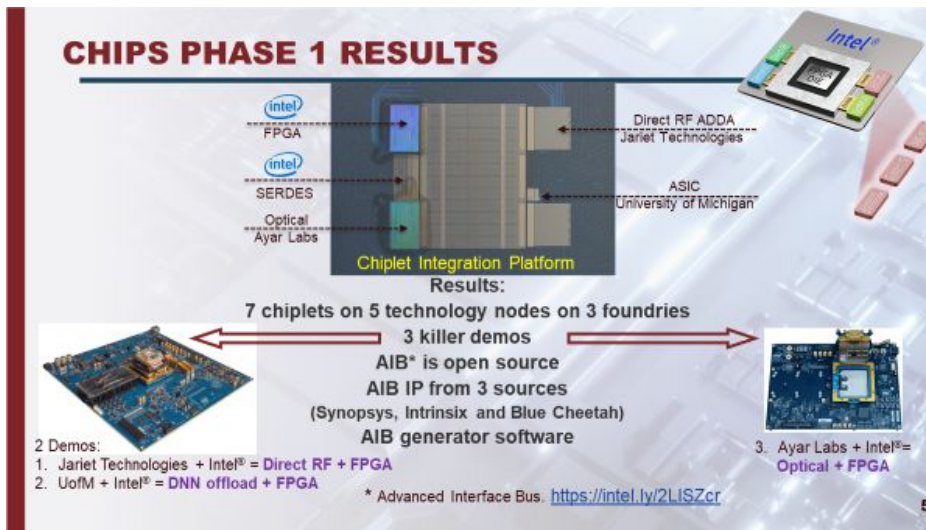


Need for Proximate
Memory with a High BW
Low Power Interface

Escape from Reticle
Limits

Additionally, yield resiliency and time to market advantages make
on-package HI attractive

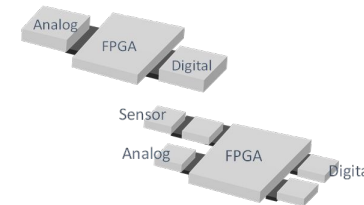
Interesting Use Cases



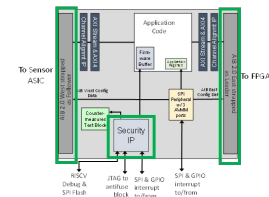
Intel Wins US Government Advanced Packaging Project
Oct 2020

... new paths for the U.S. government's industry partners to develop and modernize the government's mission-critical systems while taking advantage of Intel's U.S. manufacturing capabilities.

Multichip Prototypes:



Chiplet Design



Sources: Intel & ERI Summit (2020). The CHIPS work is supported by the DARPA MTO office (DARPA CHIPS Program))

Part of a Broad Industry-Wide Roadmap

Heterogeneous Integration Roadmap (HIR)



Launched 10-10-2019

24 chapters

590 Pages

Free download

Download Link

<https://eps.ieee.org/technology/heterogeneous-integration-roadmap>

- Sponsored by 3 IEEE Societies (EPS, EDS & Photonics) together with SEMI & ASME Electronics & Photonics Packaging Division
- Comprehensively covering microelectronics technology ecosystem
- Articulates state-of-the-art Advances in Technology & Science, Future directions, Significant roadblocks & Potential solutions
- HIR is the Knowledge Roadmap & Knowledge Supply Chain for the Heterogeneous Future



Heterogeneous Integration Roadmap

An Application Driven Roadmap

Market/System Applications

- High Performance Computing & Data Center
- Mobile
- Medical, Health & Wearables
- Automotive
- IoT
- Aerospace & Defense

Heterogeneous Integration

Components

- Single Chip and Multi Chip Integration (including Substrates)
- Integrated Photonics
- Integrated Power Electronics
- MEMS & Sensor integration
- 5G Communications & Beyond

Cross Cutting Technologies

- Materials & Emerging Research Materials
- Emerging Research Devices
- Test
- Supply Chain
- Security
- Thermal Management
- Reliability (new chapter for 2021)

Integration Processes

- SiP
- 3D +2D & Interconnect
- WLP (fan in and fan out)

Co-Design & Simulation

- Co-Design & Simulation – Tools & Practice



Summary



- Moving forward, advanced packaging will be crucial for the evolution of microelectronics systems.

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